= iSTORMY =

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Deliverable Report

D3.2 – Report on the high-fidelity modelling of the PE interface incl. Digital Twin

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Publishable summary

The iSTORMY project aims at developing an interoperable and modular Hybrid Energy Storage System (HESS) by demonstrating various use cases and seamlessly interfacing the grid to provide multiple services. In this deliverable the high-fidelity modelling of the power electronics interfaces of the HESS is detailed. This includes the interfaces from ZIG and PT to connect the high-energy and high-power batteries to the grid. The modelling framework is presented, going from high-fidelity switch modelling to passive components modelling and scaling it up at system level, based on the development of the respective low-level controllers. The high-fidelity physics-based switch modelling includes static and dynamic performance, loss modelling and thermal profiling. Results are presented and conclusions are drawn at power stage for the full HESS.

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1 Introduction

The iSTORMY project aims to develop an interoperable and modular Hybrid Energy Storage System (HESS) by demonstrating various use cases and seamlessly interface the grid to provide multiple services, such as a combination of load levelling, frequency regulation, and provision of backup power at minimum cost. The HESS consists of two battery types, high power and high energy, and two distinct power electronics interfaces to connect them to the grid.

In order to optimize the operation and maintenance of the system, a Digital Twin (DT) modelling framework is developed. This report presents the high-fidelity physics-based modelling and control design for efficient and modular PE interfaces. This includes the two PE interfaces (see D1.1) modelling along with designing the low-level controllers of the power electronics interfaces. The modelling framework is presented, going from high-fidelity switch modelling to passive components modelling and scaling it up at system level, based on the development of the respective low-level controllers. Due to the lack of experimental data from testing on the actual power electronics interfaces (confidentiality, delay), no data-driven modelling is implemented in this report. The physics-based switch modelling includes static and dynamic performance, loss modelling and thermal profiling. Results are presented and conclusions are drawn at power stage for the full HESS.

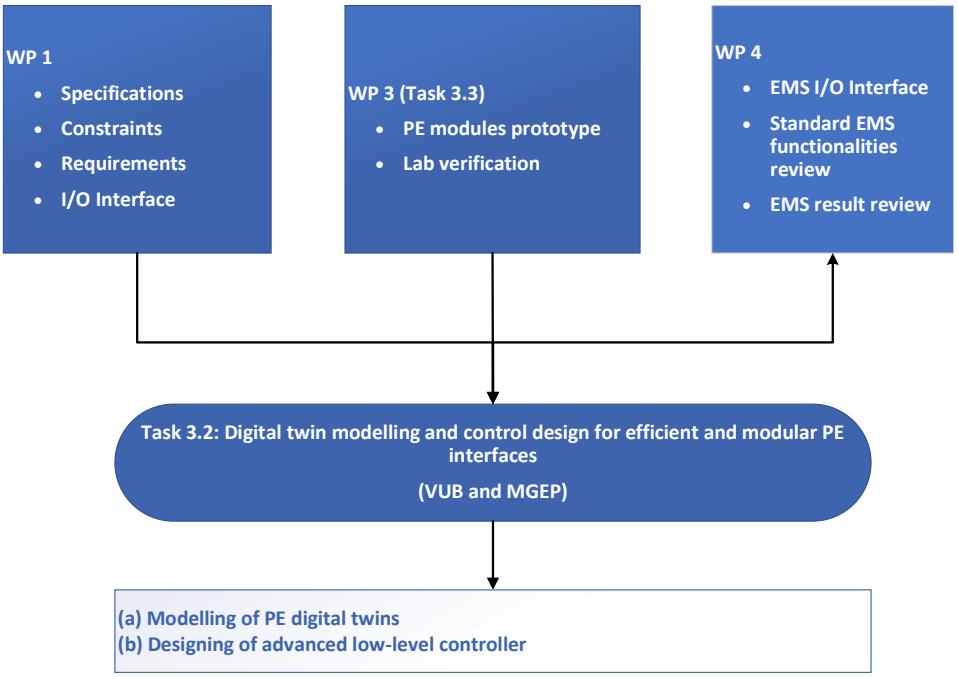


Figure 1. Interaction between Task 3.2 and other WPs (i.e., WP1, WP2 and WP4)

2 Digital twin modelling framework

The modelling of the full PE interface, see Figure 2, will be considered. As a reminder, the high-power and high-energy battery packs are connected to the grid using PRODRIVE TECHNOLOGIES (PT) and ZIGOR (ZIG) interfaces. The interface from PT comprises three modules in parallel, each with three stages, as detailed in Section 3. The interface from ZIG comprises two stages, one of which is modular with 2 modules in parallel, as detailed in Section 4. Each power stage low-level controller has a specific control functionality, as detailed in Section 5.

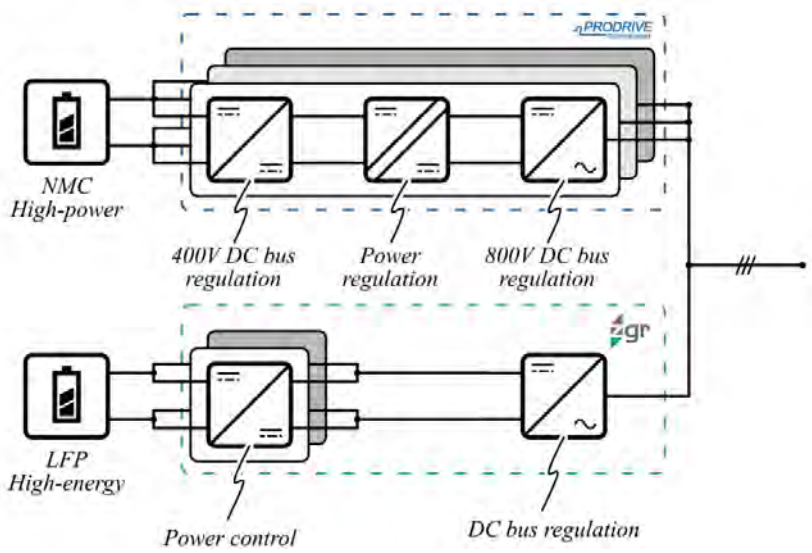


Figure 2. PE modules topology for both battery branches.

The DT modelling aims to capture the dynamics of the physical PE system towards loss estimation and junction temperature estimation so that operational degradation can be assessed in Task 3.4 (Physics-based failure mechanism and function safety of the PE modules), and real-time operation can be closely monitored in the self-healing Energy Management Strategy (EMS), Task 4.2, during physical asset operation. The DT framework comprises three parts: (1) component stage modelling, (2) power stage or system level modelling and (3) data-driven DT modelling. As shown in Figure 3, the modelling outcome of the first stage is used for the system-level modelling to capture the dynamics in parallel with the physical PE interface. The data from these dynamics of the PE interfaces is fed into a data-driven modelling routine to replicate as closely as possible the physical PE interfaces behavior and generate a DT.

To characterize the PE interfaces of the HESS as defined in Task 1.1 in terms of data, physics-based detailed modelling is carried out and their dynamics are recorded, also as input to Task 3.4. The characterization is required for faster and long-term simulation to access the PE lifetime degradation for different use cases as well as in the deployment of twin in the edge or cloud computing infrastructure. The modelling of the DT for two PE interfaces for high power (HP) and high energy (HE) battery pack of HESS along with adaptive low-level controllers (LLC) is discussed in the following sections. However, only high-fidelity physics-based modelling is detailed in the report due to the lack of experimental testing data on the PE converters. Switches and passive components are considered first, low-level controllers next, and finally, the system-level modelling is detailed.

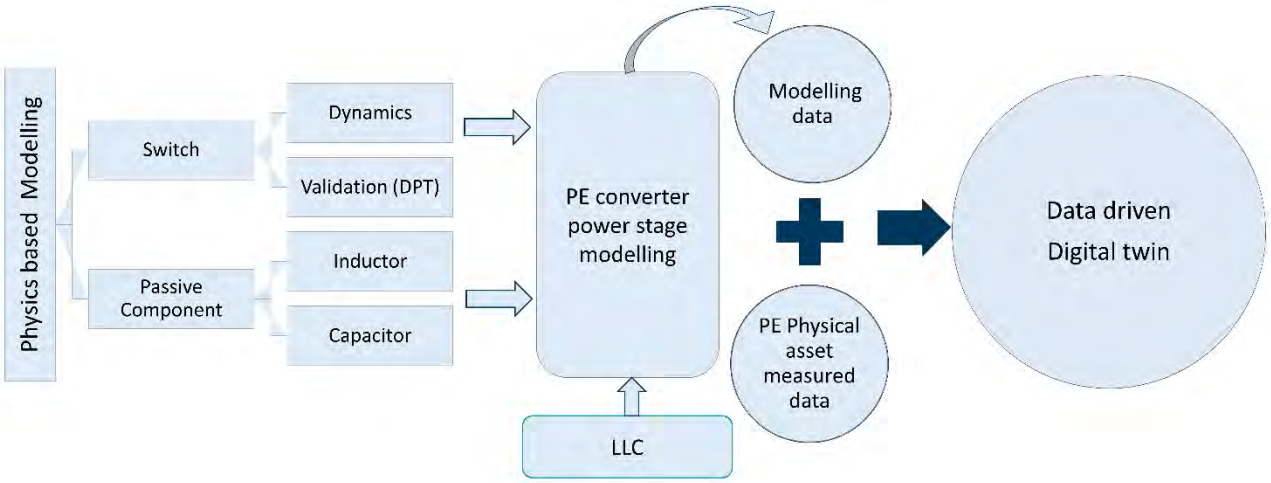


Figure 3. Conceptual building block for DT modelling

3 PT PE interface components modelling

The PT PE interface is used to connect the HP battery pack to the grid, with three modules in parallel. Each module is composed of three power stages, as shown in

Figure 4. The PE interface includes silicon carbide (SiC) power-switching technology for high efficiency (approx. 98%). The PT PE interface comprises three bidirectional power stages and two types of SiC switching technologies for low voltage (switches S1) and high voltage (switches S2) regulation in the DC and AC sides. From the battery side, a half-bridge step-up converter (100V to 400V) is connected to a dual active bridge for isolating the DC-DC stage, followed by a two-level standard AC/DC converter (800V to 400V) stage. As indicated in

Figure 4, each power stage is also operated with different switching frequencies. The significant components of these power stages are modelled to capture the dynamics and attributes of the system-level operation. This will be used at a later stage together with data-driven modelling to generate the full Digital Twin.

The modelling of the switches is presented first followed by the modelling of the interface passive components.

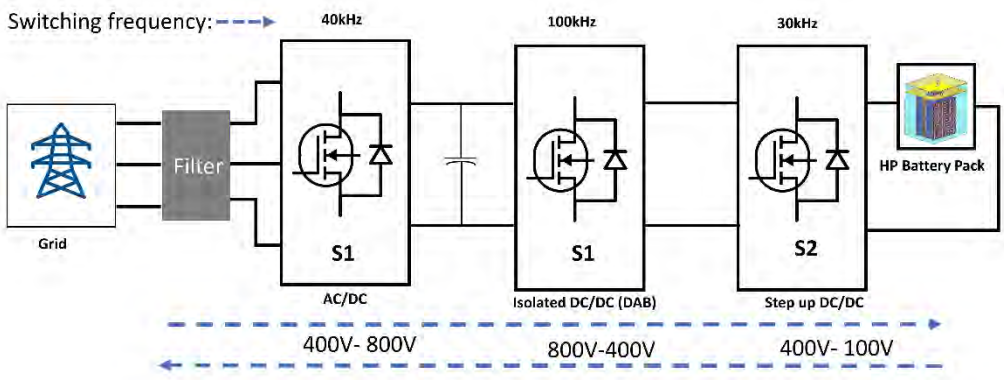


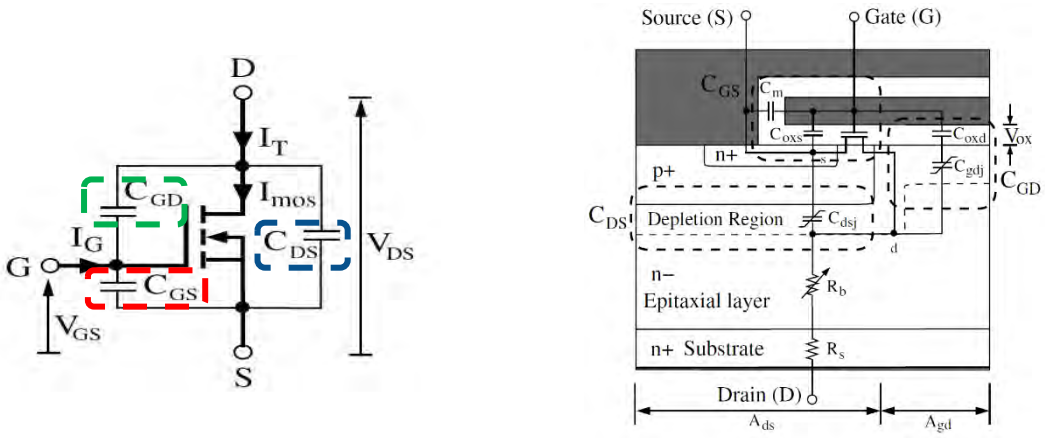
Figure 4. PT PE interface connecting the HP battery pack to the grid.

3.1 Switches Modelling

The switch modelling is considered with physics-based modelling to characterise the static and dynamic performance. The physics-based dynamic behaviour of the switch is modelled in relation to its internal capacitances, MOSFET current (I_{mos}), drain current (I_{DS}), gate current (I_G), gate-source voltage (V_{GS}), and drain-source voltage (V_{DS}). The modelling framework presented below is valid for both switches (S1 and S2), which are also referred to as MOSFET technology. Information and data are drawn from the actual switches' datasheets.

3.1.1 SiC switch general modelling

As shown in the physical MOSEFET layout in Figure 5, the capacitances between the terminals of the device gate-source capacitance (CGS) and gate-drain capacitance (CGD) govern its switching behaviour because they must be charged and discharged by the gate drive circuit during turn-off and turn-on operations. The drain-source capacitance (CDS) also governs the switching speed. These capacitances are composed of internal capacitances shown in Figure 5(b). They are gate-source oxide capacitance C_{oxs}, source metallization capacitance C_m, gate-drain oxide capacitance C_{oxd}, gate-drain depletion capacitance C_{gdj}, and drain-source depletion capacitance C_{dsj}. The C_{gdj} and C_{dsj} capacitances of the device increase as the thickness of the voltage blocking layer decreases and simultaneously decrease the effective series resistance R_b because of the expansion of depletion in the voltage blocking layer while keeping the series drain resistance R_s at a constant value.



(a) (b)

Figure 5. Intrinsic view of SiC Power MOSFET device (a) Internal equivalent capacitances (b) network outlook of cross–section area [1].

The static behavior of the switch is modelled with the relation between MOSFET current I_{mos} and drain-source voltage, V_{DS} using Eq. (1)-(3) as in [2] to characterize the real switch.

$$I_{\text{mos}} \cong \begin{cases} I_{\text{DSat}}(1+\lambda V_{\text{DS}})\left(2-\dfrac{V_{\text{DS}}}{V_{\text{DSat}}}\right)\dfrac{V_{\text{DS}}}{V_{\text{DSat}}} \text{ for } V_{\text{DS}} < V_{\text{DSat}}\text{: linear,} \\ I_{\text{DSat}}(1+\lambda V_{DS}) \text{ for } V_{\text{DS}} \geq V_{\text{DSat}}\text{: saturation,} \end{cases} \tag{1}$$

$$I_{\text{DSat}} = B(V_{\text{GS}} - V_{\text{T}})^n \tag{2}$$

$$V_{\text{DSat}} = K(V_{\text{GS}} - V_{\text{T}})^m \tag{3}$$

where V_{DSat} denotes the drain saturation voltage, I_{DSat} the drain saturation current, V_T the threshold gate voltage, and λ the channel length modulation factor. Parameters B and n regulate the characteristics in the saturation region while K and m regulate in the linear region. These parameters are extracted using the search iteration algorithm discussed in [3].

The internal capacitances of the power MOSFET, shown in Fig. 4(a), are the broadly influential factor for the switch dynamic behavior. Nevertheless, the values of these capacitors depend on the variable depletion capacitances and constant MOS layer capacitances as shown in Figure 5(b). The SiC power MOSFET is governed by these capacitances [4] that can be derived using equations (4) to (6) as a two-point representation.

$$C_{iss}(v_{ds}) = C_{gs}(v_{ds}) + C_{gd}(v_{ds}) \tag{4}$$

$$C_{oss}(v_{ds}) = C_{ds}(v_{ds}) + C_{gd}(v_{ds}) \tag{5}$$

$$C_{rss}(v_{ds}) = C_{gd}(v_{ds}) \tag{6}$$

where C_{iss} is the input capacitance, C_{oss} is the output capacitance, and C_{rss} is the reverse transfer capacitance.

Please note that the other important factor influencing the switching behavior of a power MOSFET is the gate resistor along with the parasitic inductances. These factors affect switching time, switching losses, and reverse recovery of freewheeling diode [5], and in the digital twin modelling, these parameters act as fitting response parameters as these parameters vary in applications.

Furthermore, the device's physical temperature dependency is considered through modelling parameters such as threshold voltage and transconductance in agreement with the available datasheet for the selected device. The above parameters' values change according to the temperature, affecting the model current-voltage behavior [6].

3.1.2 Static performance

The switch model static performance is validated against the datasheet information, namely with constant gate–source voltage (Vgs) and sweeping drain–source voltage (Vds) at fixed temperature to get the transfer characteristics of the SiC MOSFET module. Figure 6 and Figure 7 illustrate the experimental and simulated I–V characteristics for different gate voltages for the two selected switches: high voltage regulation switch (S1) and low voltage regulation switch (S2) of PT PE interface at room temperature, respectively. It can be observed that the model shows a high goodness of fit at different gate drive voltages.

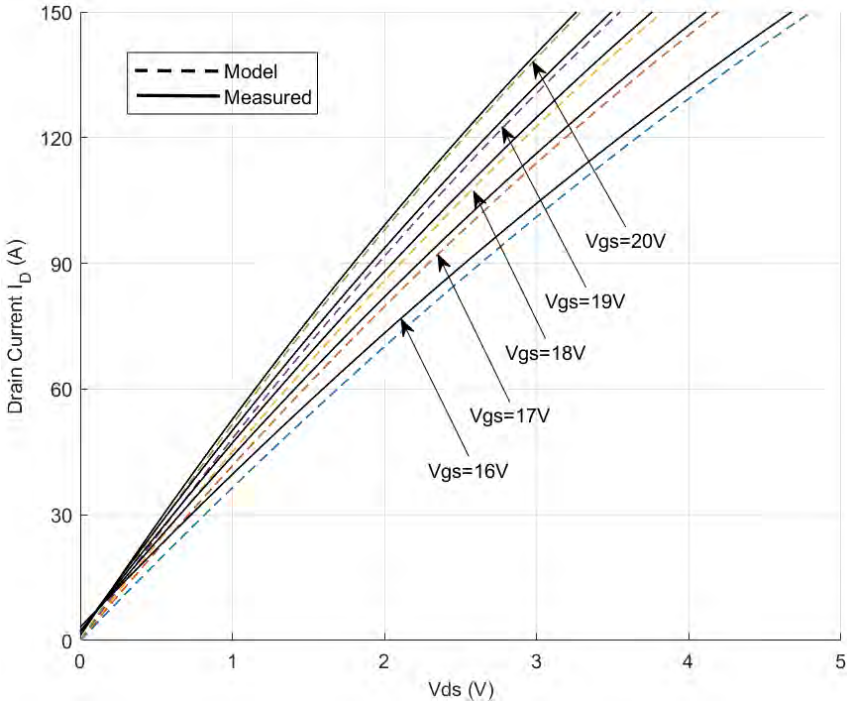


Figure 6. Drain current response with respect to drain voltage and different gate voltages at 25°C for S1.

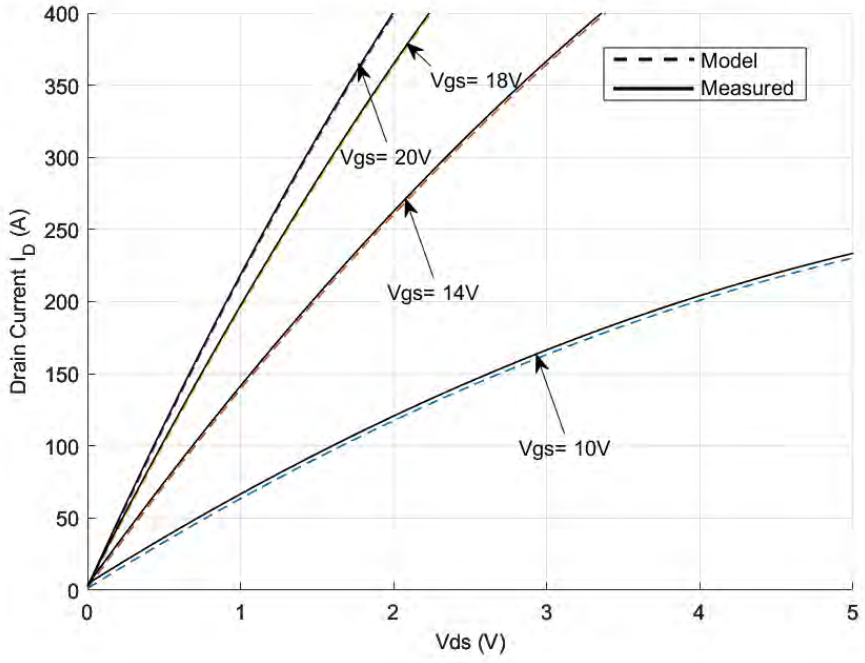


Figure 7. Drain current response with respect to drain voltage and different gate voltages at 25°C for S2: (a) excerpt of datasheet; (b) static model response.

3.1.3 Dynamic performance

The transient switching response with dynamic capacitances and parasitics is evaluated in the test circuit with a drain supply voltage (V_{dd}) and gate pulse generator (V_g) for different drain and gate voltages. The dynamic switching response of Figure 9 is evaluated with respect to Figure 8 in terms of ideal operating conditions. The switching turn-on of the MOSFET, the length of time interval and gate currents in Table 1 as well as some of the definitions of the parameters will be discussed in the next paragraphs.

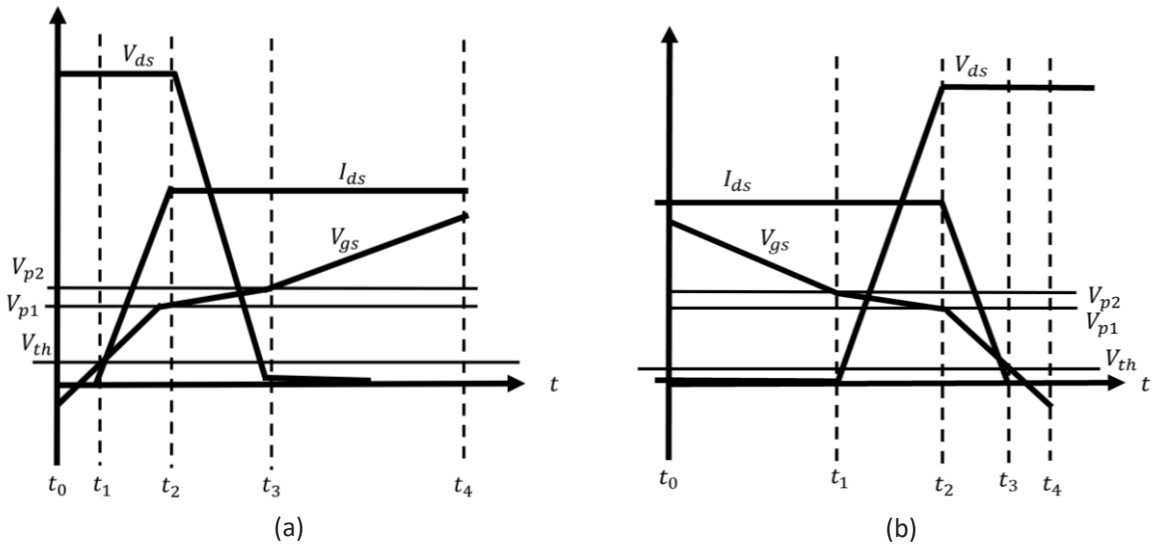


Figure 8. Switching timing sequence: (a) turn-on; (b) turn-off.

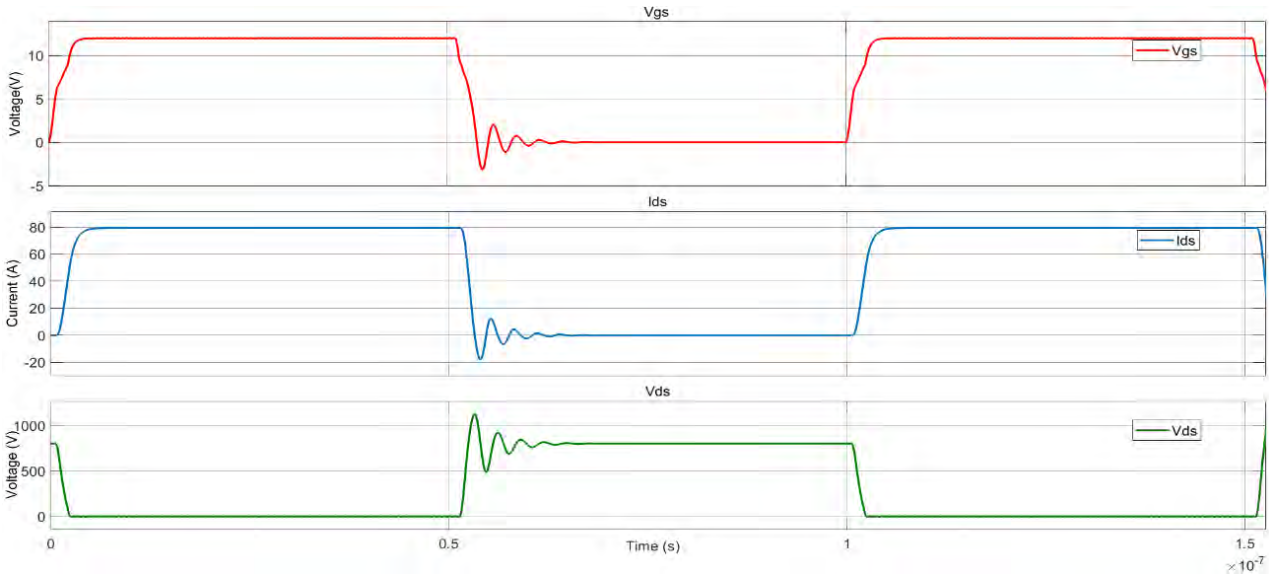


Figure 9. Dynamic characteristics of PT PE switch (S1) for Vgs, I_{ds} and V_{ds}, tested at Vds=800 V, Ids=80 A and Vgs=12 V.

In Figure 8(a), between t_0 and t_1 the input capacitance, C_{iss}, of the MOSFET will be charged until V_{gs} reaches the threshold voltage, V_{th}. As can be seen in Figure 9, the initial rise of the current with rising V_{gs} is low. So, in this model, the current only starts to rise when the gate to source voltage reaches the voltage, V_{p1}. Please note that C_{iss} can be considered constant, $C_{iss,\,high}$ for high V_{ds} and low V_{gs} which leads to use RC network for the current flowing to the gate of the switch and the time difference.

From t_1 and t_2, the gate to source voltage increases beyond the threshold voltage, $V_{th,}$ so the I_{ds} now increases significantly, and a non-flat miller plateau voltage (Vp) characteristics is seen in Figure 9 with respect to Figure 8(a). The voltage is still high, so the MOSFET is operating in the saturation region. This means that the current will approximately scale linear with the gate-source voltage, as seen in Figure 9. Since usually $V_{gs} \gg V_{th}$, the current to the gate will be assumed constant. This means that V_{gs} increases linearly with time as the input capacitance, C_{iss}, is almost constant. At time t_2, all of the load current flows through the MOSFET. This allows to estimate the energy lost in the switch during this time interval.

Between t_2 and t_3, V_{gs} will remain almost constant while V_{ds} drops. This is because of the flatness of the I_{ds} curves in the saturation region, as shown in Figure 8(a). During this interval, the reverse transfer capacitance, $C_{rss} = C_{gd}$, is discharged as V_{ds} drops. Because of the voltage dependency of C_{rss}, the voltage will not drop linearly but will have a steeper slow at t_2 than at t_3 which is found in Figure 9.

After, t_3, v_{gs} will rise towards the applied final gate voltage $V_{gs}+$. During this time, the on-resistance of the MOSFET will be lowered.

Table 1: Gate current and time differences for the switching on transient in Figure 8(a) [7].

Timing	**Gate current (I_g)**	**Time difference (Δt)**
t_o - t_1	$\frac{V_{gs-} - V_{gs+}}{R_g + R_{g\_int}} e^{\frac{-t}{(R_g + R_{g\_int})C_{iss}}}$	$-(R_g + R_{g\_int})C_{iss} ln(1 - \frac{V_{th} - V_{gs-}}{V_{gs+} - V_{gs-}})$
t_1- t_2	$C_{iss} \frac{V_{gs+} - 0.5(V_p - V_{th})}{I_g})$	$C_{iss} \frac{V_p - V_{th}}{I_g})$
t_2- t_3	$\frac{V_{gs+} - V_{p)}}{R_g + R_{g\_int}}$	$\frac{Q_{gd}(C_{rss})}{I_g}$
t_3-t_4	Drain current is in saturation region so no time difference is considered	

Under the same assumptions as the ones that are discussed in the turn-on transient, the timings and gate current are derived and given in Table 2. However, during the turn-off process, once the gate-source voltage Vgs decreases to the threshold gate voltage V_T, the drain current I_D begins to decrease, and the drain-source voltage V_{DS} also begins to increase to the drain voltage supply V_{dd} as noticeable in Figure 9 . During the final turn−off interval, V_{gs} falls below 0 V to discharge C_{iss} fully. As the estimated V_T is only ~2.3 V to fully discharge C_{iss}, V_{gs} goes to a negative voltage, confirming the S1 simulation model response according to the physics.

Table 2: Gate current and time differences for the switching on transient in Figure 8(b) [7]

Timing	**Gate current (I_g)**	**Time difference (Δt)**
t_o - t_1	$\frac{V_{gs-} - V_{gs+}}{R_{g,off} + R_{g\_int}} e^{\frac{-t}{(R_g + R_{g\_int})C_{iss}}}$	$-(R_g + R_{g\_int})C_{iss} ln(1 - \frac{V_{gs+} - V_p}{V_{gs+} - V_{gs-}})$
t_1- t_2	$\frac{V_{gs-} - V_{gs(mp)}}{R_{g,off} + R_{g\_int}}$	$-\frac{Q_{gd}(C_{rss})}{I_g}$
t_2- t_3	$C_{iss} \frac{V_{gs+} - 0.5(V_p - V_{th})}{I_g})$	$-C_{iss} \frac{V_{gs(mp)} - V_{th}}{I_g})$
t_3-t_4	At this stage the drain current reaches the saturation region, so no time difference is considered	

As discussed for S1, the dynamics of switches S2 are presented in Figure 10. It depicts that the turn-on process begins when the gate drive voltage rises to 12 V. The gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} are charged with the current passing through the gate series resistance R_g and the gate series inductance, including

parasitic L_g. When gate-source voltage V_{gs} continues to increase from the threshold gate voltage, V_{th} to the Miller plateau (V_p), the drain current I_D begins to increase and the drain-source voltage V_{DS} also begins to decrease to $I_{ds} \cdot (R_b + R_s)$.

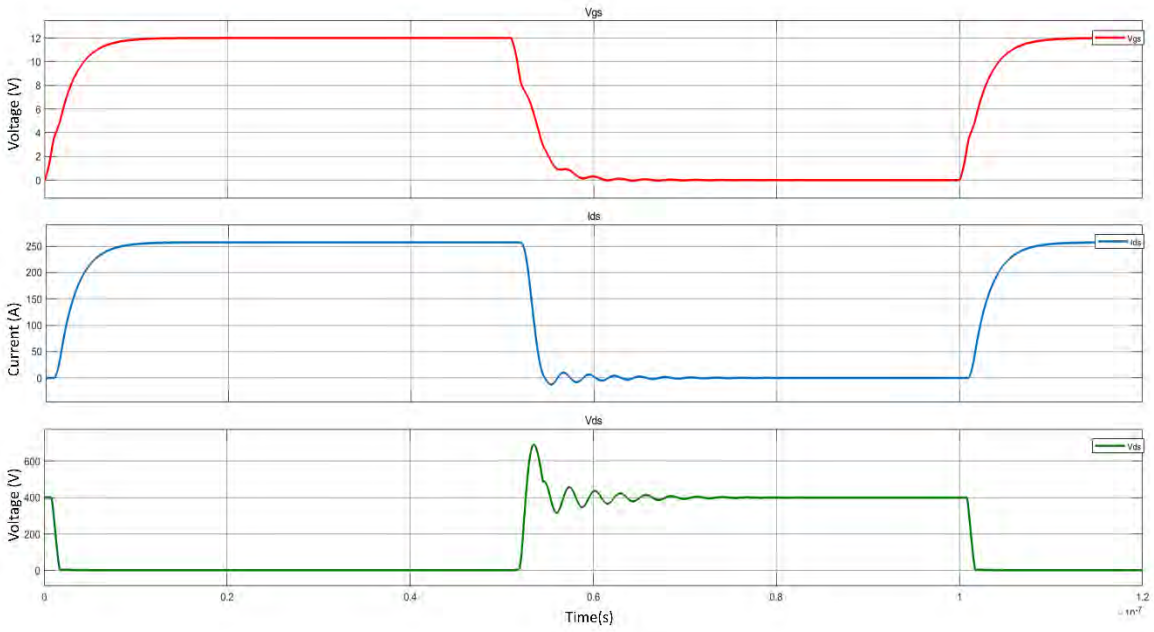


Figure 10. Dynamic characteristics of PT PE low side switch (S2) for V_{gs}, I_{ds} and V_{ds}, tested at Vds=400 V, Ids=250 A and Vgs=12 V.

3.1.4 Loss modelling

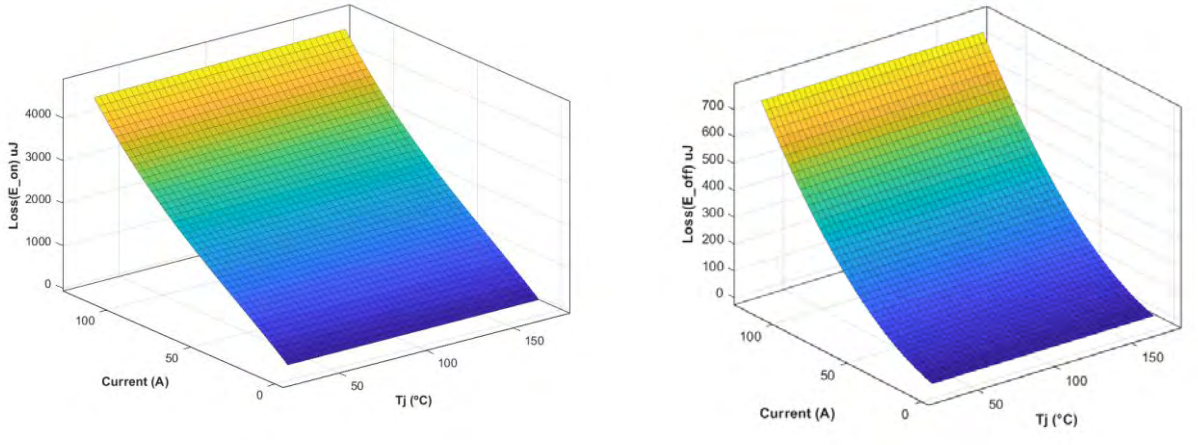
The loss modelling is derived using the previous switch models by considering realistic device load current, voltage variations, switching frequency and ambient temperature. The device model estimates the voltage drop across the device and the switching energies as a function of the current, the off-state blocking voltage, and junction temperature. Furthermore, the extracted parameters and the switching frequency are used in the power loss (P_{Loss}) model where the device's instantaneous conduction and switching losses are calculated. The switching losses for S1 and S2 are shown in Figure 11 and Figure 12, respectively. The losses are related to the off-state blocking voltage V_{DD}, the instantaneous drain current I_D, the switching frequency f_{SW} and the junction temperature T_j. They are calculated using equation (9).

$$P_{SW} = \left(E_{on} + E_{off}\right) \cdot f_{SW} \tag{7}$$

The conduction losses estimation is carried out using the drain-source on-state resistance $(R_{D\,on})$ using equation (8). When the device is fully on, the only electrical resistance is represented by the resistance of the structure. This resistance is due to many contributions, especially the temperature reported in the datasheets.

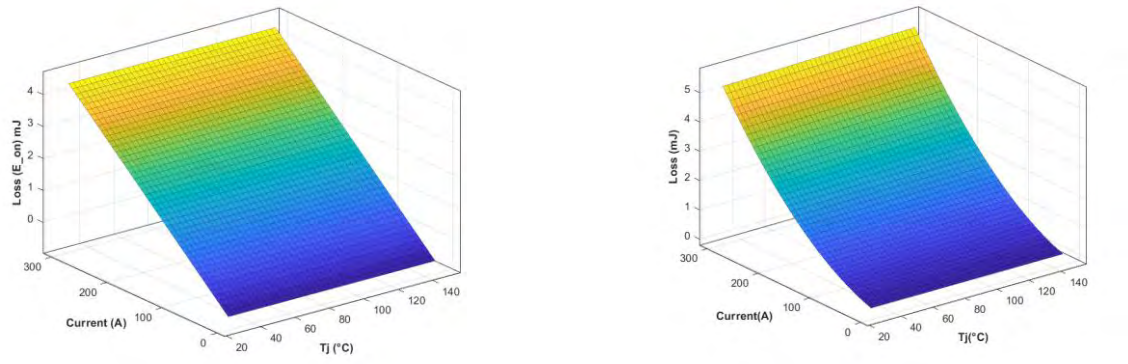
$$V_{DS}(i_D) = R_{DSon}(i_D) \cdot i_D \tag{8}$$

where V_{DS} and i_D are drain-source voltage and drain current, respectively.



(a) (b)

Figure 11. Switching losses for the high voltage regulation switch (S1).



(a) (b)

Figure 12. Switching losses for the low voltage regulation switch (S2).

The conduction losses of the anti-parallel diode can be estimated using a diode approximation with a series connection of the DC voltage source (V_{D0}) representing diode on-state zero-current voltage and a diode on-state resistance (R_D), V_D being the voltage across the diode and i_F the current through the diode:

$$V_D(i_D) = V_{D0} + R_D \cdot i_F \quad (9)$$

3.1.5 Thermal profiling

Thermal stress is evident when the switch is in operation due to electrical power dissipation. Thermal profiling is considered with a classical approach rather than using Cauer and Foster models. The classical approach is simple yet insightful in terms of thermal response pattern recognition, whereas other methods deal with more robust mechanisms but have cons such as limited information availability; converter building parasitics variance affects the accurate thermal network parameters estimation [9]. The thermal profiling approach is shown in Figure 13 and the total thermal resistance is summarized by equations (10) and (11).

Please note that losses and stress vary due to different parasitic parameters, which means that actual hardware performance tests will be fed as fitting factors where necessary.

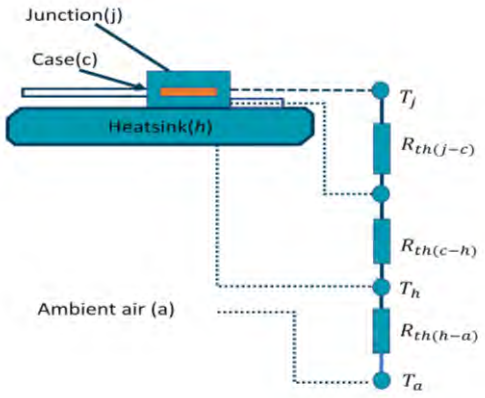


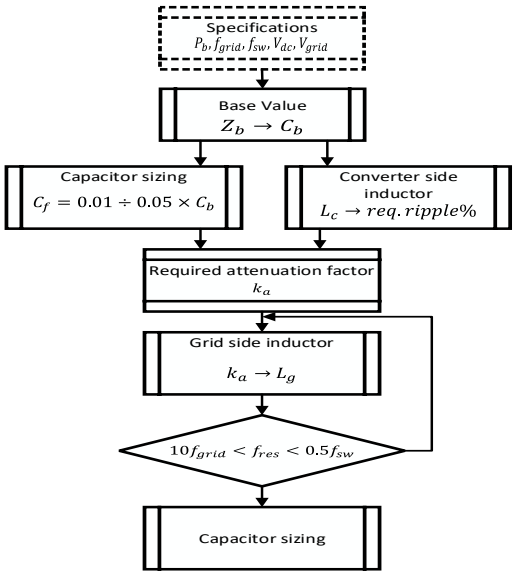
Figure 13. Thermal profiling approach for switch modelling.

$$R_{th(j-a)} = R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)} \quad (10)$$

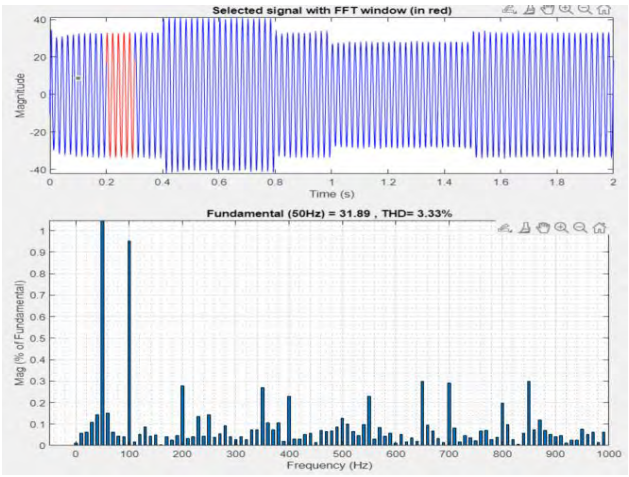
$$T_j - T_A = P_D\left(R_{th(j-c)} + R_{th(c-h)} + R_{th(h-a)}\right) \quad (11)$$

3.2 Passive components modelling

The passive components, especially in the grid-connected filter, are highly important for ensuring the power quality. A second order filter is widely adopted in grid-connected interfaces for BESS. However, the high switching frequency of SiC MOSFET directly impacts the inverter's output filter performance, so based on the defined switching frequency for PT two-level standard inverter, the parameters of the LCL filter are considered using the algorithm in Figure 14(a). For the algorithm, the known equations from (8-9) are adopted. For the calculations a 20% allowed ripple in terms of attenuation factor has been considered along with the 5% base capacitor value. Also, to ensure stable frequency a passive damping resistance is calculated. The parameters are reported in Table 3. The quality of the grid injected current is shown in Figure 14(b) with a THD under normal operation of 3,33%. With undervoltage the THD is 4,05% and it is 2,52% with overvoltage, which shows the proper system operation.



(a)



(b)

Figure 14. Second-order filter: (a) parameters calculation algorithm; (b) THD while injecting grid current during normal operation.

Table 3: Filter parameters for PT grid connecting PE interface.

Parameters	Value
Gride side inductance	0.012 mH
Inverter side inductance	0.70 mH
Filter capacitance	24.86 uF
Damping resistance	0.23Ω

The goal of this section is to model high-performance inductors having high relative permeability with low eddy current using the available data of the vendors and estimating inductor losses accurately. As for the DC-link capacitor, it is selected with low equivalent series resistance (ESR) to reduce ripples and temperature rise in output voltage. Estimation of ESR is considered during the capacitor loss estimation and modelled in (12) while considering temperature as drying out factor which is subjected to high ripple currents and therefore more heat in circuit function. The behavioural map of the ESR used for PT PE interface is shown in Figure 15.

$$ESR = \frac{R_2}{1 + (2\pi f)^2 C_2^2 R_2^2} + R_1 + R_0 \tag{12}$$

where R_0 is resistance of foil, tabs, and terminals in ohm (Ω); R_1 is the resistance of electrolyte in ohm (Ω) ; R_2 is the dielectric loss resistance (Ω) ; and f is the switching frequency.

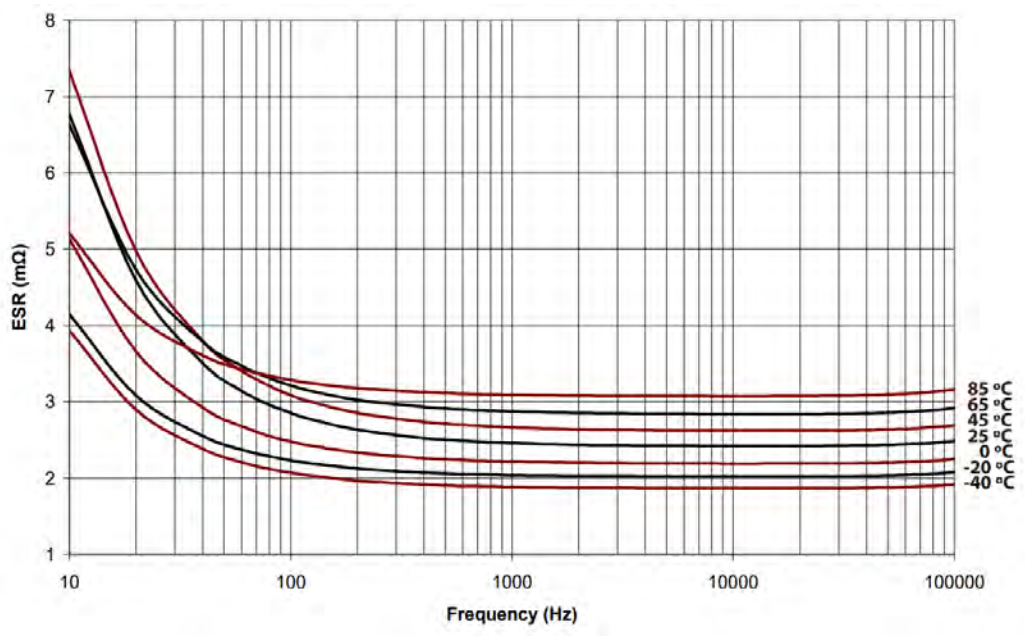


Figure 15. Behaviour of ESR as function of frequency and temperature.

The inductor losses are comprised of core losses P_{fe}, air-gap losses P_{gp} and copper losses P_{cu}. Rectangular HF 299 Litz wire is used to wire the inductor. The inductor copper losses P_{cu} can be calculated as equation (13):

$$P_{cu} = R_{Lz} I_{L,RMS}^2 \tag{13}$$

where R_{Lz} is the resistance of Litz wire and $I_{L,RMS}$ is the root mean-square current of the inductors.

The Improved Generalized Steinmetz Equation is used to estimate the inductor's core losses and gap losses as equations (14)-(16). The parameters are accumulated from the vendor datasheet.

$$P_{fe} = W_t(k_{ns}, k, f_{sw}^{y}, \Delta B_{max}^{x}) \quad (14)$$

$$P_{gp} = k_g \cdot k \cdot c. l_g \cdot f_{sw} \cdot \Delta B_{max}^{x} \quad (15)$$

$$\Delta B_{max}^{x} = \frac{0.4\pi NF\left(\frac{\Delta I}{2}\right)10^{-4}}{l_g + \left(\frac{MPL_{cm}}{\mu_m}\right)} \quad (16)$$

where W_t is the weight of the core material, k_{ns} and k are the loss coefficients for non-sinusoidal waveform and C-shaped core material, f_{sw} is the switching frequency, B_{max} is the maximum flux-swing at the rated condition, x and y are core material parameters, k_g is the coefficients for gap loss, c is the core depth factor, l_g is the air-gap coefficient, N is the number of turns, F is the core packaging factor, ΔI is the since it offered decidedly smaller ESR, the high capacitance current ripple, l_g is the total gap length, MPL is the mean per volume, low voltage ripples, and temperature rise. path length is in cm, and μ_m is the material characteristics.

The expression for calculating the DC-link capacitor losses is obtained from (17), where $I_{C,\,RMS}$ is the root mean-square current value of the DC-link capacitor and ESR is capacitor equivalent series resistance, which is frequency dependant and shown in Figure 15.

$$P_{loss\,C} = I_{C,RMS}^{2}(t)ESR(f) \quad (17)$$

4 ZIG PE interface components modelling

The ZIG PE interface is used to connect the HE battery pack to the grid as a non-isolated power stage topology. It is made of two buck/boost DC/DC power converters at the battery side and a three-phase two-level AC/DC power converter at the grid side, as shown in Figure 16. Both converters are bidirectional and include SiC switching technology. As shown in Figure 16, the switching frequency is 35kHz for both converters with a common DC link.

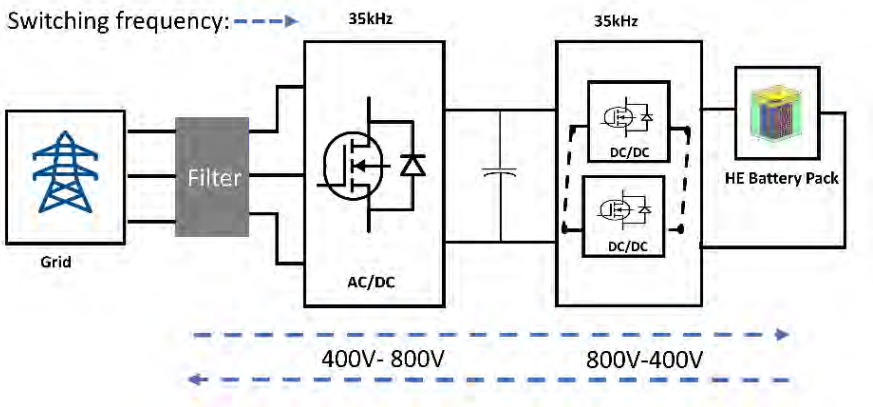


Figure 16. ZIG PE interface connecting the HE battery pack to the grid.

4.1 Switch modelling

The switch technology used in this interface follows the same modelling approach as for PT PE interface which has been discussed in the previous section. In this section the model data for different high-fidelity attributes are reported.

In terms of static performance, the device model which has been discussed in section 3.1 validation has been achieved by comparing the simulation results and OEM datasheet measured values, the model on-state characteristics shown in Figure 17 are fairly in agreement while the switching current is increased from 0A to 120A as per the OEM measured values for different gate voltages at 25°C. Please note that the selected switch for both power stages of ZIG have the rating of 1.2kV voltage, 115A current at 25°C with 16mOhm $R_{ds(on)}$. The model responses due to the effects of different junction temperatures (Tj) on the switching on-state behavior at a fixed gate voltage are shown in Figure 18. Figure 19 shows the estimated switching energy losses while different junction temperatures are produced. For the DT,

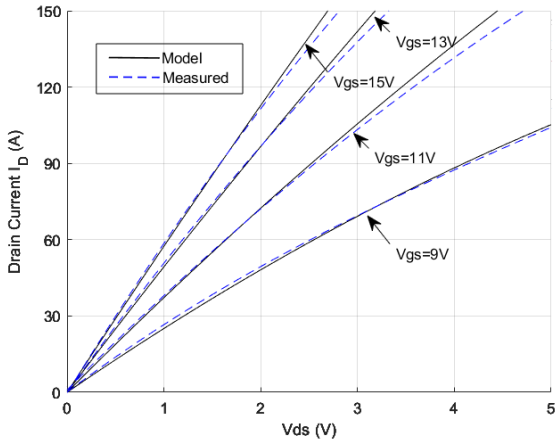


Figure 17. Static performance with relation to drain current, drain voltage and different gate voltages at 25°C

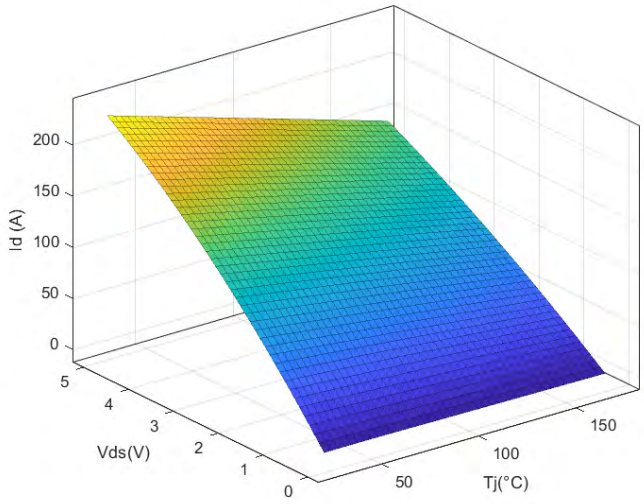
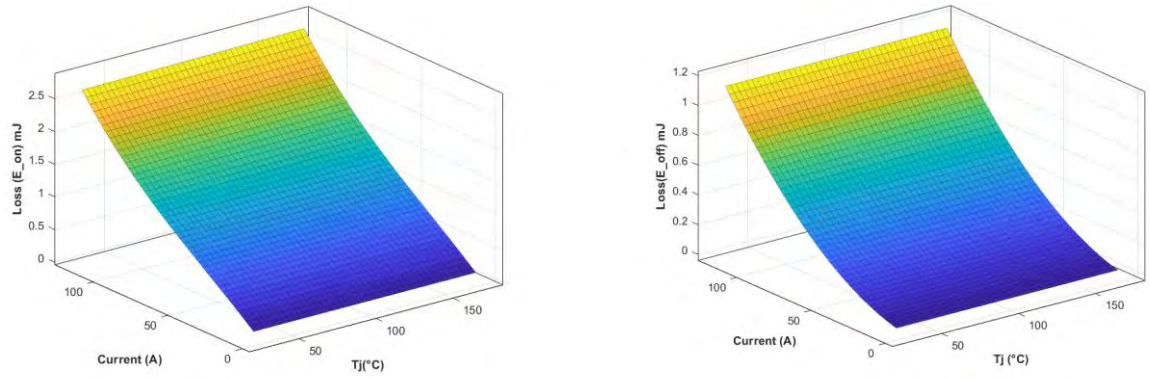


Figure 18. Drain voltage-current behaviour at different junction temperatures.



(a) (b)

Figure 19. ZIG semiconductors switching losses

4.2 Passive components modelling

The passive components in ZIG PE interface are modelled similarly to those of PT, as discussed in section 3.2. The values have been provided by ZIG and are reported in Table 4.

Table 4. Passive components parameters for grid interfacing PE interface.

Parameters	Values
DC-link capacitor	114 uF
AC filter capacitor	15 uF
Snubber Cap	0.015 uF
Filter Inductor	300-400 uH

5 Advanced low-level controllers

In this section the development of the adaptive low-level controllers (LLCs) for the PE interface converter modules is described. The LLCs will interact with the energy management strategies (EMS) being developed in WP4. The LLCs will ensure that the PE modules operate with appropriate dynamics and damping in the three use cases of the project (refer to D1.1 for more details).

As illustrated in Figure 2, each stage in the converter topology requires a specific LLC to fulfil the specific required functionalities, which include controlling the intermediate DC buses and regulating the active and reactive power exchanged with the grid according to the setpoints defined by the upper-level EMS.All the models, controls and simulations have been carried out in Matlab/Simulink. It must be noted that the converters have to be controlled to exchange a certain amount of power based on the grid service to be provided, so they require an algorithm to synchronise with the grid. In this case, the synchronisation algorithms of both converter topologies are classical phase locked loops (PLLs) based on a synchronous reference frame aligned with the voltage at the point of common coupling (PCC). Moreover, it must be mentioned that the controller gains have been first tuned by trial-and-error, although a genetic algorithm is being implemented to obtain an optimal control gain set to improve the dynamic response and stability margins of the converter.

5.1 HP battery branch LLC

The HP branch is comprised by three modules in parallel, having within each one a boost converter, a dual active bridge and a two-level inverter.

As shown in Figure 2, the Boost converters are responsible for setting the low-level DC link, which is carried out with classical PI-based regulators.

The power references calculated instantaneously by the EMS are fed to the DAB power controllers, which regulate the transferred power by modifying the phase difference between the two active bridges.

In the last stage of the converters, the inverters are equipped with a low-level current controller implemented in a rotating *dq* reference frame. A feedforward term has been included in each control loop to compensate for the coupling terms that appear in the reference frame transformation. Moreover, the voltage at the point of common coupling has been feedforwarded to reduce the control burden of the current PI regulators. On top of this current controller, a DC bus voltage regulator has been included to establish the high-level dc voltage of the converter through the current in the *d* axis. The implemented control structure of the inverter can be observed in Figure 20 Since in the use cases established in D1.1 there is no requirement to regulate the exchanged reactive power, in this case the current in the *q* axis is set to zero. However, a more advanced reactive power regulator is being developed in the framework of T4.4. to carry out the upscaling of the proposed LLC.

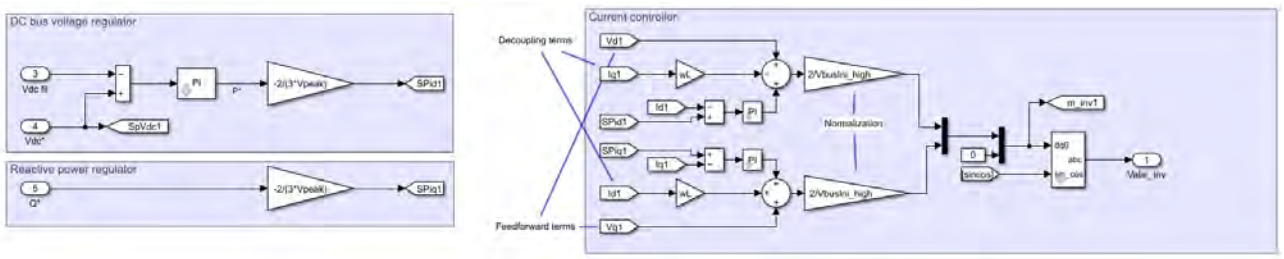


Figure 20. HP branch's inverter control.

5.2 HE battery branch's LLC

The HE converter topology is comprised by a unique module that includes two boost converters in parallel and a single inverter. The difference with respect to the HP converter is that there is no intermediate DAB converter to step-up the voltage. Since both converter stages are the same as those pf the HP interface, the basic control of both is very similar to the one described in Section 5.2. The difference in this case is that the inverter, instead of regulating the DC bus voltage, is responsible for controlling the power exchanged with the grid. In addition, the Boost converters are responsible for regulating the exchange of power with between the ESS and the grid.

5.3 Results of the LLC implementation

The LLC of both branches have been tested under active power setpoint step-shaped variations. First, each converter has been tested individually to fine-tune the control parameters, and once configured, the entire converter topology has been simulated. As an example, Figure 21 shows the time-domain evolution of the active power in the dual active bridge of one of the parallel modules of the HP converter. This power corresponds to the power exchanged between the converter and the grid.

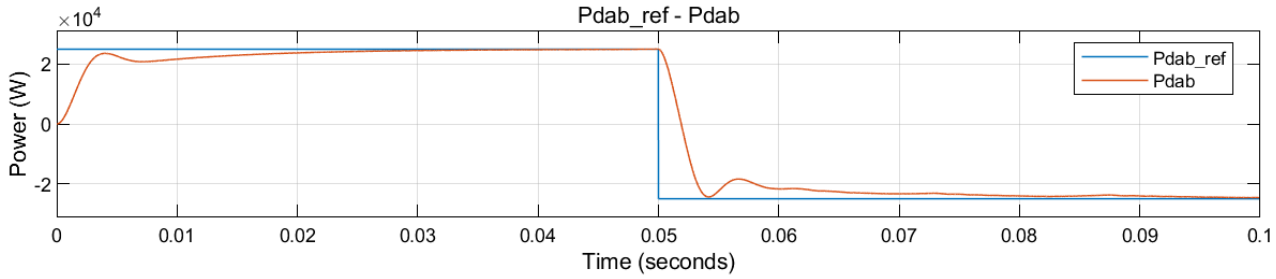


Figure 21. Active power step (in blue) and real active power (in orange) in the dual active bridge of the first PE module of HP branch.

In the following figure, the time-domain evolution of the inverter variables can be observed. The I_d current reference varies to regulate the high-side DC link voltage to its predefined value, which is modified by the power transferred by the dual active bridge. On the other hand, the current I_q is regulated near to 0 because the reactive power setpoint is set to zero.

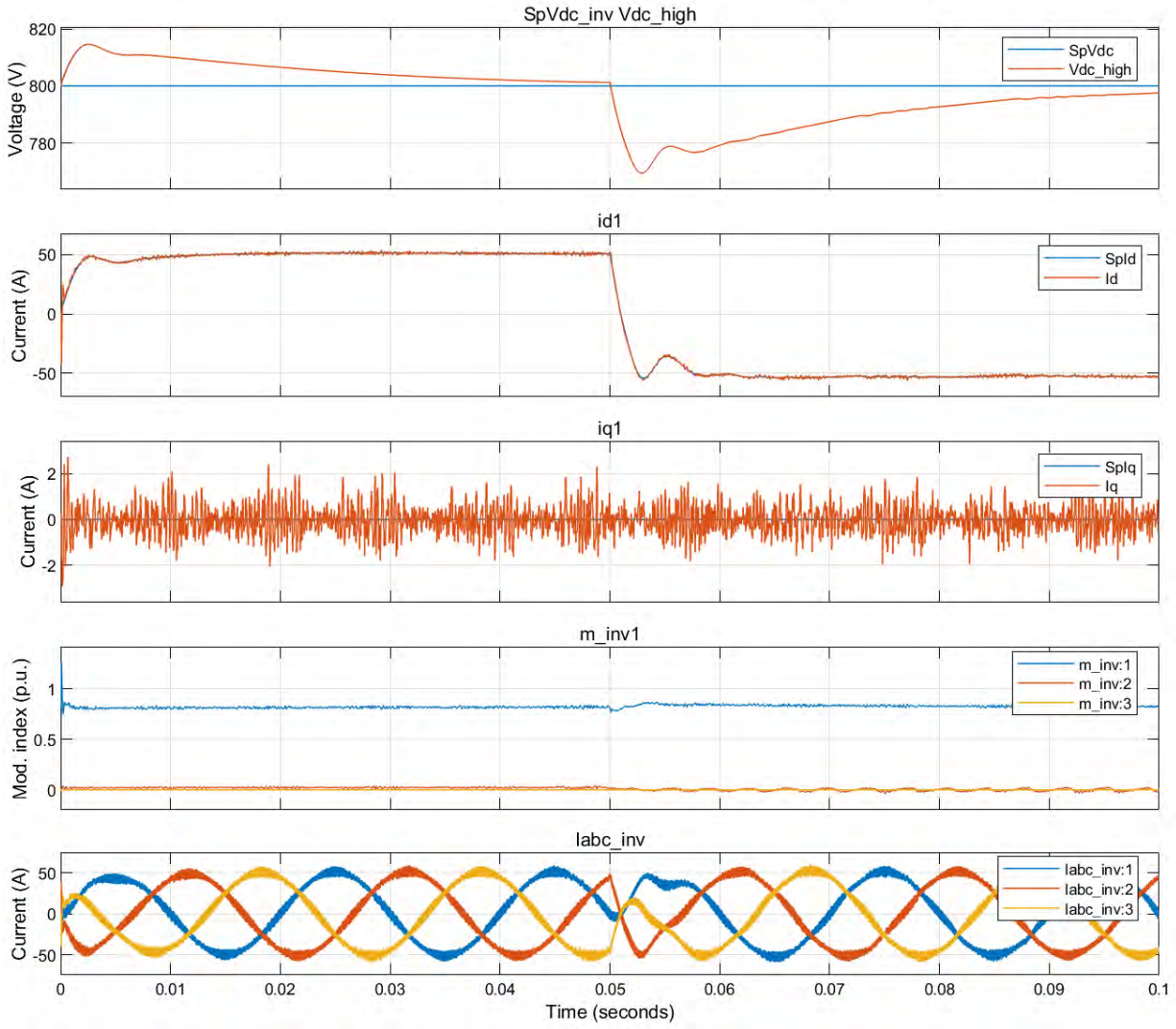


Figure 22. Some parameters of the inverter of the first PE module of HP branch.

Regarding the HE interface, the results in Figure 23 exhibit a similar behaviour. As mentioned above, the main difference is that the Boost converters are responsible for regulating the exchanged power, whereas the inverters control the voltage at the DC link through the current in the *d* axis.

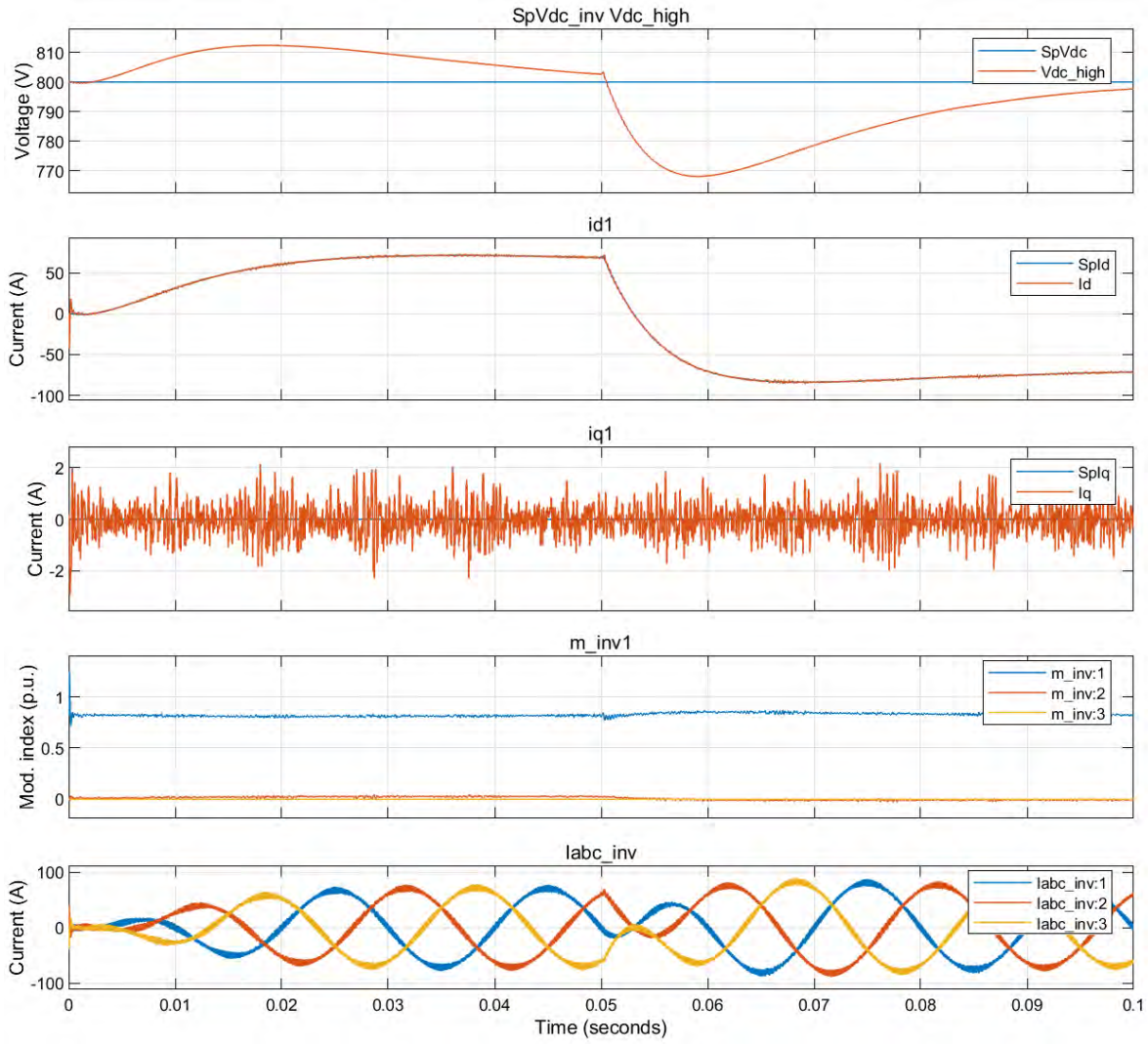


Figure 23. Some parameters of the inverter of the HE branch.

Once the converters are tested individually, the entire converter topology has been simulated to ensure that the designed LLC structure adequately controls the active power exchange. Figure 24shows the complete simulation model comprised by three HP converter modules from PT in parallel with the ZIG HE converter.

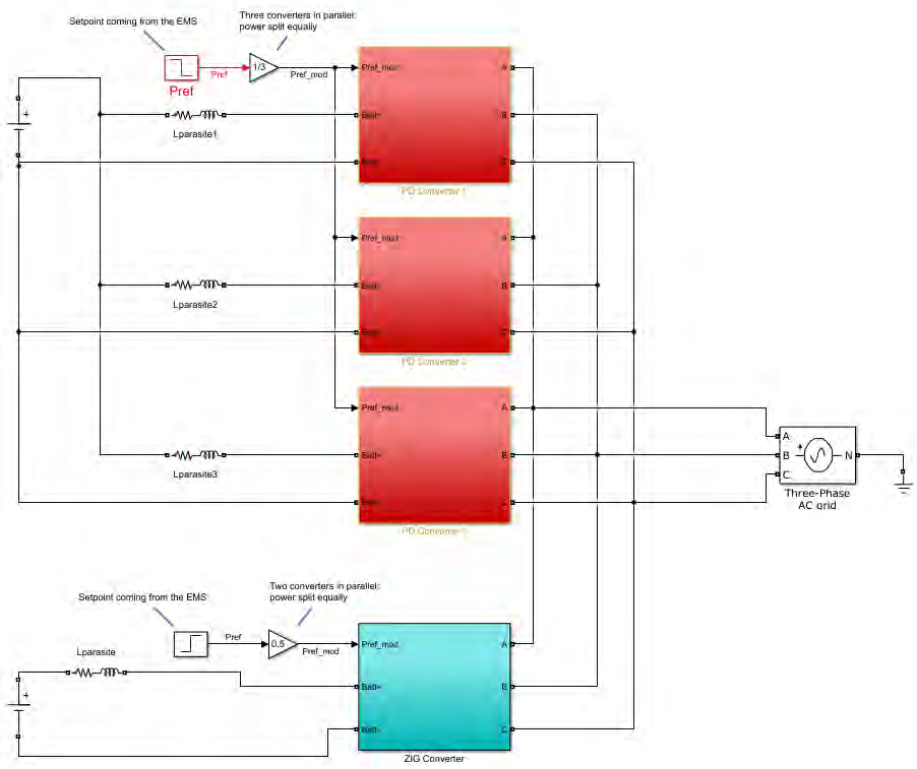


Figure 24. Complete converter simulation model to test the LLC

The following figure illustrates the time-domain evolution of the power provided by these converters for step-shaped variations in the power setpoints. The HP modules have the same setpoint, so their exchanged power is almost equal. Regarding the HE module, it can be observed that there is a brief transient where the converter absorbs active power from the grid to establish the DC link voltage. Once the bus voltage is regulated, the exchanged power is regulated based on the setpoint coming from the upper-level EMS.

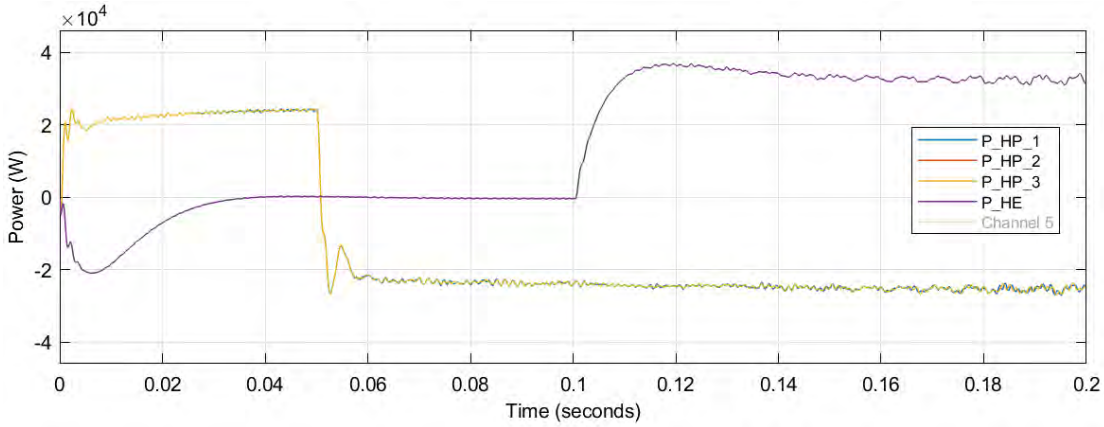


Figure 25. Exchanged active power of the entire converter topology

6 Power stage modelling

The power stage modelling requires grid side PE interface response and battery pack side PE interface response. These power stage response data from the model along with PE physical asset test data will be fed to the data driven model. The PE converter stage is comprised of high-fidelity switches models, detailed passive components modelling and advanced control strategies which has been discussed in the previous sections. The following sections discuss the ZIG PE interface response for different power stages with details since PT PE interfaces response are discussed in Section 5. By using the above information, the PE power stage modelling dynamics are recorded for DT framework and reported in the sections below.

6.1 ZIG power stage

The ZIG PE interface is comprised of two stages: buck/boost DC/DC converter for interfacing battery side to ensure the bi-directional energy transfer and a two-level inverter interface for grid connection while participating in the defined use cases. The ZIG system consists of two modular DC/DC converters with a 15kW rating connected to a common DC-bus. The grid connection to the grid is made using a 30kVA inverter. The battery side converter modelling responses along with the LLC in section 5 are shown in Figure 26 against the request active power while the battery starting SOC is at 40% with a defined HE battery pack voltage. The bidirectional AC/DC inverter dynamics in responses- DC-link voltage, grid side voltages, and inverter currents to the same power request have been presented in Figure 27. After the change in the power set-point, it took 16ms for the DC-link to reach its desired value. Moreover, the voltage ripple remained under 3% of the nominal voltage along with the defined LLC. The PE interface baseplate temperature is estimated in terms of power dissipation by considering thermal impedances in combination with forced air colling and heatsink for the system level. The baseplate temperature is preferred to ease hardware data acquisition and validation with the estimated result. The estimated temperature for different power stages is show in the Figure 28.

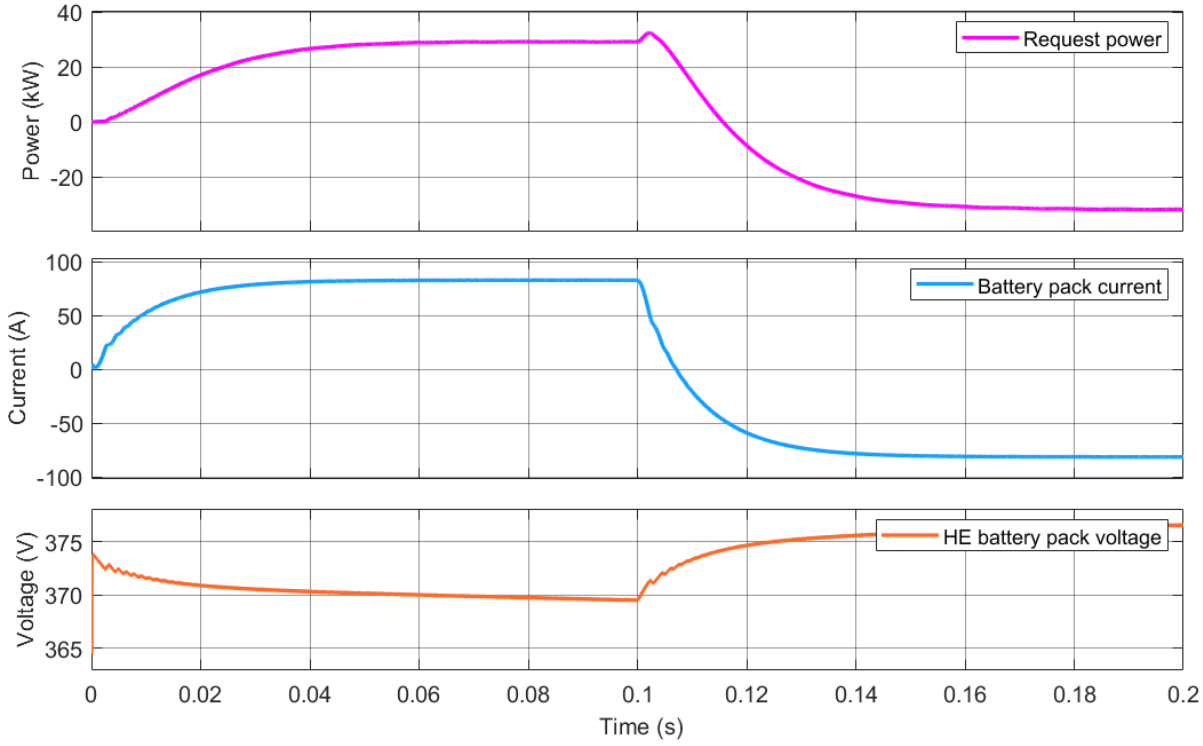


Figure 26. ZIG DC/DC power converter stage dynamics.

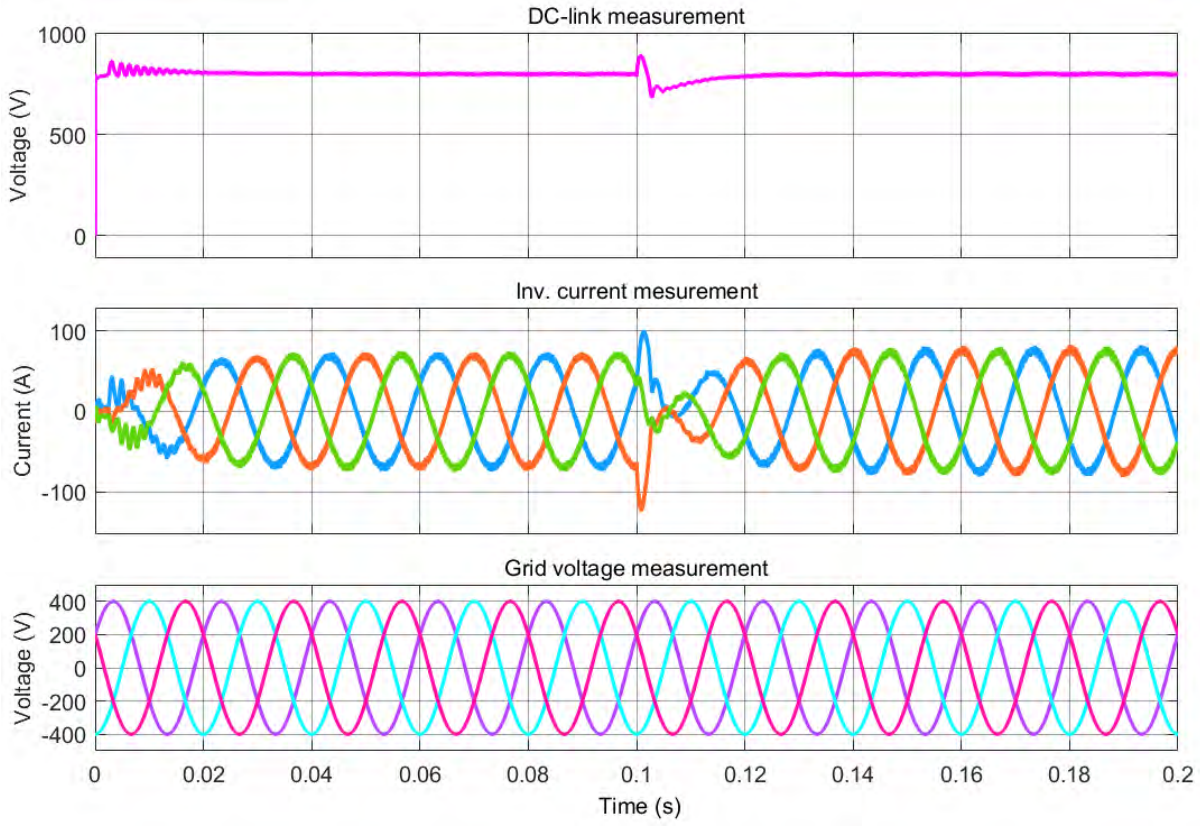


Figure 27. ZIG AC/DC power converter stage dynamics.

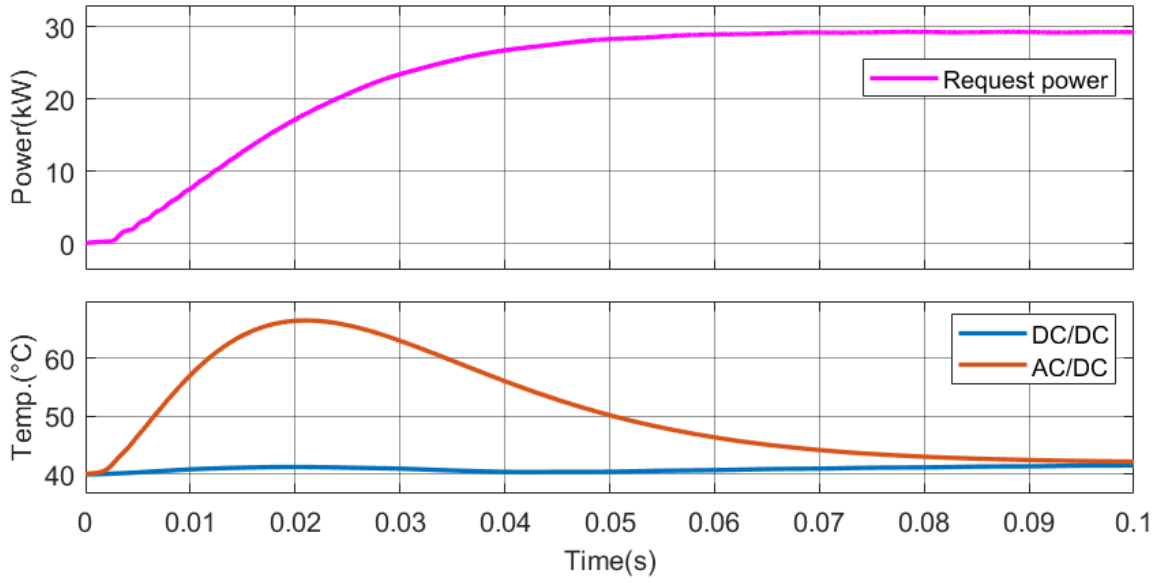


Figure 28. ZIG PE interface temperature dynamics.

6.2 PT power stage

The PT power stage modelling responses and required dynamics for DT have already been discussed in parallel with advanced low-low controller strategies. The baseplate temperature attribute for the complete PT PE interface has been measured against the exact power profile dynamics used in the LLC control design for PT interface. The base temperature is also measured in terms of power loss incorporating the thermal impedances in combination with the forced air cooling and heatsink; and an initial ambient temperature of 40°C. The variation of the temperature with respect to the transferred power in three stages is shown in Figure 29.

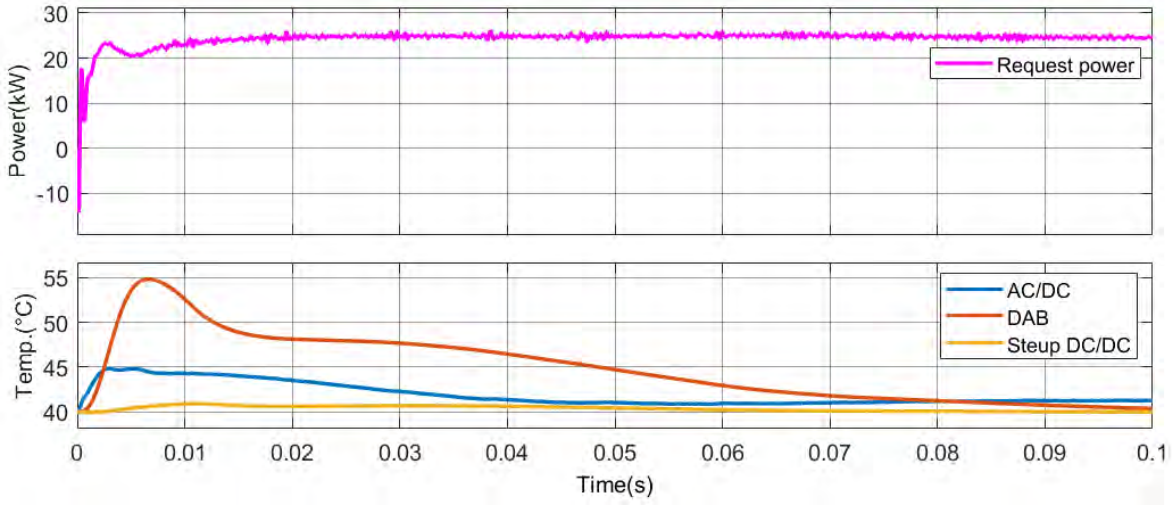


Figure 29. PT PE interface temperature dynamics in three stages.

7 Conclusions

In this report the Digital Twin modelling framework as defined in Task 3.2 has been detailed for the PE interfaces, considering physics-based components and system-level modelling. In particular, the switches used for both PT and ZIG interfaces have been modelled with high-fidelity, considering static and dynamic performances, loss estimation and thermal profiling. The passive components have also been modelled. The low-level controllers have been developed for the different converters of both interfaces, in order to provide the required functionalities. The combination of the LLCs and components modelling led to physics-based system-level results for the two interfaces.

Due to the lack of experimental testing data from the converter prototypes, no data-driven modelling is prepared as part of this task. Testing data is expected to be available to some extend in the coming months of the project and will be used in the frame of the reliability modelling in Task 3.4, also extending the Digital Twin modelling with data-driven models.

8 Risk Register

Risk No.	What is the risk	Probability of risk occurrence[1]	Effect of risk[1]	Solutions to overcome the risk
4	Lack of aging/degradation data for PE modules	High	DT modelling not fully data-driven, fewer actual data for T3.4 & WP4 (out)	Use already available data and extrapolate from datasheets
5	Confidentiality of data from the OEMs	High	DT modelling not fully data-driven, lower model accuracy	Close collaboration between the partners to find alternatives to potentially confidential data

[1)] Probability risk will occur: 1 = high, 2 = medium, 3 = Low

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Project partners:

#	Partner short name	Partner Full Name
1	VUB	VRIJE UNIVERSITEIT BRUSSEL
2	PWD	POWERDALE
3	CEG	CEGASA ENERGIA S.L.U.
4	CEA	COMMISSARIAT A L ENERGIE ATOMIQUE ET AUX ENERGIES ALTERNATIVES
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